11-260932



## DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] Especially this invention relates to the semiconductor device which has the boundary region in which laminating formation of the different layer insulation film on a wiring layer is carried out about a semiconductor device, and a wiring repeat field is adjoined, and a circuit pattern does not exist.
[0002]
[Description of the Prior Art] Although the semiconductor device forms the wrap layer insulation film for the wiring layer pattern, it may constitute this layer insulation film from a different insulator layer which carried out the laminating depending on the case. For example, in the field of the semiconductor memory to which the manufacture yield is falling with detailed-izing of an element pattern or a circuit pattern, the redundant configuration which replaces a poor memory cell, a poor line, or a poor train with a reserve element is adopted. Generally, in case these poor memory cells are replaced by the reserve element, it is carried out by melting a fuse by the laser beam etc. and changing circuit connection. If a thick insulator layer exists on a fuse when forming this fuse in a lower layer wiring layer, it will become difficult for the energy of a laser beam to be absorbed by the insulator layer, and to melt a fuse completely. On the other hand, if the fuse is exposed, although fusing is easy, with the moisture into which it was invaded in the device, a fuse will short-circuit and reliability will fall.
[0003] For this reason, it is desirable to form the insulator layer of suitable thickness on a fuse, and it is carrying out setting management at the thickness which is about 1000A. And in order to make management of this thickness easy, the insulator layer on a fuse is formed in two-layer in the former. That is, drawing 3 is the cross section showing the example, after it forms an impurity range 2, the isolation oxide film 3, gate oxide-film 4a, and gate electrode 4b and forms a transistor on a silicon substrate 1, forms the TEOS(tetrapod ethoxy run) BPSG film 5, and performs heat treatment aiming at flattening. Then, about 2000A of tungsten silicide films used as a lower layer wiring layer is formed on the TEOSBPSG film 5, and fuse 6X which processes a predetermined configuration and consists of a part of lower layer wiring 6 is formed.
[0004] Then, about 1500A of silicon oxides 7 is formed, about 5000A of TEOSBPSG films 8 is formed on it, and the layer insulation film of a laminated structure is formed. furthermore, the contact for connecting the upper wiring layer, a ground, or a lower layer wiring layer if needed, after performing heat treatment aiming at a surface reflow -- a hole -- well-known photolithography technology -- opening -- carrying out -- this contact -- about 9000A of aluminum wiring layers is formed in the field containing a hole, and the upper wiring layer 9 is formed Furthermore, the protective coat 10 aiming at a moisture-proof disposition top is formed in the whole surface, in the etching process which carries out opening of the protective coat on the aluminum pad outside drawing, the insulator layer on the aforementioned fuse 6X is **********ed, and opening 11 is established.
[0005] In establishment of this opening 11, the etching rate of the TEOSBPSG film 8 is a part for 600-700A/, and while you can manage the thickness on fuse 6X easily and you prevent disclosure of fuse 6X since a silicon oxide 7 functions as a kind of stopper even when etching time is somewhat too long temporarily, since the etching rate of a silicon oxide 7 is a part for 400-500A/, let fusing of the fuse by the laser beam be an easy thing.
[0006]
[Problem(s) to be Solved by the Invention] however, the wiring layer which the thermal contraction of the silicon oxide 7 is carried out by difference of the rate of a thermal contraction of the TEOSBPSG film 8 and a silicon oxide 7 etc., stress works in the lower layer wiring layer 6 with this shrinkage force, and a lower layer wiring layer is moved in the direction of a flat surface in the heat treatment process at the time of the reflow in such a semiconductor memory, and adjoins, for example, contact, -- a hole may be approached or contacted and it may connect with it too hastily electrically In the semiconductor memory in which a sense amplifier, the register section, and the decoder section are prepared in the form which adjoins a memory cell field, it is easy to generate especially a phenomenon such in the edge of a memory cell field, i.e., the edge of the field in which the pattern of the same configuration is prepared repeatedly.
[0007] According to examination of this invention person, the shift amount by stress was as large as the edge of a repeat pattern, and by the inside of a pattern space the pattern which is about 15 is repeated, although not generated, in the edge of this repeat pattern, that a shift amount, large moreover, tends to shift a more long and slender pattern made most shifts clear. As this reason, since the field where the pattern which has the function which eases stress does not exist spreads out, the outside of a repeat pattern space thinks because the generated stress is making it act and shift to the pattern of an edge directly. And a shift amount is

gradually considered to decrease and go as stress is eased one by one and it goes to the interior of an edge shell, when the pattern of this edge shifts.

[0008] moreover -- a repeat pattern space -- contact -- an up-and-down wiring layer and an up-and-down ground are connected by the hole, and the role which fixes this contact hole pattern to a ground is played however, contact -- if the interval of a hole is large -- a portion in the meantime -- a shift -- generating -- the shift amount -- contact -- it is thought that it increases according to the distance from a hole for this reason -- general -- contact -- it is thought that it is easy to shift the more long and slender pattern with which the portion in which a hole does not exist becomes long

[0009] Drawing 4 is the plan of an example of a repeat field, and drawing 5 is the BB line cross section. The long and slender circuit patterns 6A-6C are established by tungsten silicide on the transistor. contact which is fixed to these wiring by the ground -- the hole is not prepared Moreover, the left-hand side of drawing is a field repeatedly, and it becomes the wiring with which circuit pattern 6C is repeatedly located in the edge of a field. And the latus field which does not have the pattern of this layer in the right-hand side of this circuit pattern 6C spreads out. moreover, the contact which consists of aluminum wiring 9 of the upper layer connected to an impurity range 2 among circuit patterns 6B and 6C -- the hole is prepared

[0010] In such a semiconductor device, the state where the circuit pattern shifted with stress is shown in drawing 6 . In this drawing, circuit patterns 6B and 6C have shifted rightward. consequently, circuit pattern 6B -- contact -- a hole 9 will be approached extremely and it will short-circuit depending on the case

[0011] In order to prevent the shift of the circuit pattern by this stress, a slot is intentionally established in the insulator layer of a ground, and there is technology which fixes wiring by making a part of wiring invade into this Mizouchi. For example, as shown in the plan of drawing 7 (a), and CC line cross section of (b), what is indicated by JP,4-348054,A used contact puncturing technology for the BPSG film 23 formed on the field oxide film 22 of a silicon substrate 21, and provides the wiring layer 25 for the slot 24 **** and on it. Since a part of the inferior surface of tongue has invaded in a slot 24, this wiring layer 25 can fix the position.

[0012] However, with this technology, if the lower layer wiring layer 26 grade exists in the lower layer of the part which forms a slot 24, since the wiring layer 25 will turn into this lower layer wiring layer 26 being easy to short-circuit, it becomes difficult to form elements, such as a transistor, in the slot 24 bottom. Since the element is arranged very densely, forming a slot in such a part makes the degree of integration of a semiconductor memory fall remarkably in the sense amplifier especially described above, the register section, and the decoder section.

[0013] The purpose of this invention is to offer the semiconductor device which the shift of the circuit pattern in the edge of the repeat field of a circuit pattern is prevented, and can prevent faults, such as short-circuit of a circuit pattern.

[0014]

[Means for Solving the Problem] this invention is characterized by equipping the field contiguous to the edge of the repeat field of a circuit pattern with a circuit pattern and the dummy pattern of this layer in the semiconductor device by which the circuit pattern by which the repeat array was carried out is covered by two or more insulator layers. Two or more insulator layers of especially this invention are effective in the semiconductor device which consists of cascade screens of a silicon oxide and a TEOSBPSG film. Moreover, as for a dummy pattern, it is desirable to be formed by the same wiring material as a circuit pattern.

[0015]

[Embodiments of the Invention] Next, the operation gestalt of this invention is explained with reference to a drawing. Drawing 1 is the plan of 1 operation gestalt of this invention, and drawing 2 is the AA line cross section. In these drawings, the isolation oxide film 3 is formed on a silicon substrate 1, an element field is formed, a gate oxide film and contest polysilicon are deposited on this element field, and gate oxide-film 4a and gate electrode 4b are formed by carrying out selective etching of these. Moreover, the impurity range 2 as a source drain field is formed by introducing an impurity into a silicon substrate 1 using this gate electrode 4b, and this forms a transistor.

[0016] In an appropriate top, the TEOSBPSG film 5 is formed in the whole surface, heat treatment aiming at flattening is performed, about 2000A of tungsten silicide films which serve as a lower layer wiring layer on the TEOSBPSG film 5 after that is formed, and the circuit patterns 6A-6C and fuse 6X which process a predetermined configuration and consist of lower layer wiring 6 are formed. Then, about 1500A of silicon oxides 7 is formed, about 5000A of TEOSBPSG films 8 is formed on it, and the layer insulation film of a laminated structure is formed. furthermore, the contact for connecting the upper wiring layer, a ground, or a lower layer wiring layer to a required part, after performing heat treatment aiming at a surface reflow -- a hole -- well-known photolithography technology -- opening -- carrying out -- this contact -- about 9000A of aluminum wiring layers is formed in the field containing a hole, and the upper wiring layer 9 is formed Furthermore, the protective coat 10 aiming at a moisture-proof disposition top is formed in the whole surface.

[0017] And as shown in drawing 3 , in the etching process which carries out opening of the protective coat on the aluminum pad outside drawing, selective etching of the protective coat 10 on the aforementioned fuse 6X is carried out, the TEOSBPSG film directly under ] 8 of it is further **********ed to the necessary depth alternatively, opening is established, and it constitutes as opening 11 for fuse fusing.

[0018] In such a semiconductor device, originally, although it consists of circuit patterns 6A-6C as shown in drawing 4 , the lower layer wiring which consists of tungsten silicide in which the aforementioned fuse 6X was formed uses the circuit patterns 6D and 6E unrelated to actual circuit operation as a dummy pattern at the boundary region which spreads on the outside of the edge of a field here repeatedly using the same tungsten silicide, and is carrying out formation arrangement. With this operation gestalt, these dummy patterns 6D and 6E are the same width-of-face sizes as the aforementioned lower layer circuit patterns

6A-6C, and, moreover, are arranged in parallel.

[0019] Therefore, although stress tends to act on the lower layer wiring layer 6 by the thermal contraction of a silicon oxide 7 in the heat treatment process at the time of a reflow for formation of said upper wiring etc. according to this composition To circuit pattern 6C located in an original circuit pattern, especially the edge of a repeat field Since this is adjoined and the dummy patterns 6D and 6E are arranged, circuit pattern 6C of the edge of a repeat field which was described above will be in the state where it is not the edge of a repeat field, and the shift of the circuit pattern which is easy to produce in this edge will be prevented. This is because it is canceled that the field where the pattern which has the function which eases stress does not exist is formed in the outside of a repeat pattern space by forming the dummy patterns 6D and 6E, the stress applied to circuit patterns 6A-6C by this will be eased in the uniform state, and generating of a shift will be suppressed.

[0020] In addition, since the effect of the stress relaxation by the dummy patterns 6D and 6E will become still higher by shifting the dummy pattern itself and making stress absorb, as for the dummy patterns 6D and 6E, it is desirable to form in a narrow width as much as possible. The effect will become more effective if the ratio of a width-of-face size and linear dimension is especially set or more to 1:20. Moreover, with this operation gestalt, although it is the example which arranged two dummy patterns, it is not restricted to this number and can set up if needed. However, in a repeat field, from the place which a shift has hardly produced, a dummy pattern arranges about 20 preferably, and by the place which this invention person checked, it can prevent a 15 [ about ] shift almost completely in the inside position where 15 circuit patterns were arranged in parallel.